REMARKS

Claims 17-22 are pending and stand rejected under Section 102 in view of the Uchiyama reference (USP 6,748,507). The most recent office action also included a rejection under Section 112. As explained herein, Applicant respectfully traverses these rejections.

As the office action explains, both rejections are premised on reading certain paragraphs of Applicant's published application relating to control of an SDRAM (2004/0199716; Par. references herein refer to Applicant's published application). In particular, the Examiner cited Pars. 0027 and 0283-0301 in support of the rejections. The Examiner understood that the presently pending claims are directed to, and supported by, this subject matter.

Applicant respectfully submits that these rejections are in error and should be withdrawn.

Applicant respectfully submits that the Examiner has overlooked portions of Applicant's disclosure and the exemplary support for the presently pending claims. The presently pending claims are not directed to control of an SDRAM. The presently pending claims are directed to a data processor that operates in accordance with a plurality of operation modes based on the mode register, wherein the plurality of operation modes comprise operation modes of the data processor, and the operation mode in which the data processor operates is based on the mode register.

The support for the presently claimed invention is included in portions that the Examiner apparently did not consider. Applicant respectfully requests that the Examiner consider, for example, Fig. 4 and in particular standby control register STBYR. The Examiner's attention is directed to Pars. 0115-0122, and in particular to Par. 0120 and Table 1 of Applicant's published application.

In accordance with the present invention, the operation mode of the data processor is based on contents of the mode register (e.g., STBYR). The expressly recited operation modes that are indicated by the mode register include a first operation mode (CPU executes instructions), a second operation mode (CPU and clock pulse generator halt operation), and a third operation mode (CPU halts executing instructions and clock pulse generator generates clock signals). The portions of Applicant's disclosure cited above describe such structure and operation.

It is respectfully submitted that such portions of Applicant's disclosure, when interpreted by one of skill in the art, sufficiently support the claimed subject and distinguish Applicant's claims from the cited art. Applicant submits that construing the claims in view of Applicant's disclosure results in the claims being readily distinguishable from the cited art. The mode register of Uchiyama does not provide the relationship between the mode register and the operation modes of the data processor as claimed by Applicant. The mode register of Uchiyama does not indicate the operation modes of the data processor and is for a different purpose and does not fulfill the relationship with the operation modes recited in the presently pending claims.

Accordingly, Applicant requests that the rejections be withdrawn. Applicant's disclosure supports the claimed invention and fully comports with Section 112. Uchiyama's mode register relates to controlling the operation of the external synchronous DRAM, and Uchiyama does not disclose or suggest Applicant's invention.

If there are any questions or issues regarding the foregoing, Applicant requests an opportunity to discuss such matters with the Examiner by way of an in-person or telephone interview. No new matter has been added.

Please charge any additional fees due, or credit any overpayment, to Deposit Account No. 50-0251.

Respectfully submitted,

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I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated above.